ABSTRACT OF THE DISCLOSURE

A demodulator includes a count section, a synchronization timing setting section, and a code judgment section. The count section has four counters that count a number of waves of an FSK-modulated digital signal at different timing within a bit time width. The synchronization timing setting section designates a synchronized timing signal based on the count value of the count section. Then, the code judgment section compares the count value with a threshold value to judge the signal level, thereby decoding the digital signal.